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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/935,639	08/24/2001	Takashi Nakamura	040894-5699	1378

9629 7590 12/19/2002

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/935,639	NAKAMURA ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *17-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-16,31 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Receipt is acknowledged of paper submitted under 35 U.S.C. 119(a)-(d), from Japanese Patent Application Nos. P2000-254291 filed on August 24, 2000 and P2001-254696 filed on August 24, 2001 which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-8,13-16 and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Hayashi et al. (U.S. Patent No. 6,133,092 herein after Hayashi).

With respect to claim1, Hayashi describes a semiconductor device having an electrode formed on a surface of a semiconductor substrate, (Hayashi fig. 4 # 60 formed on substrate 51, col. 5 lines 65-67) wherein said electrode includes a barrier

layer consisting of amorphous or micro crystal expressed by an expression of $M1_x M2_{1-x}$ (0 <x<1), (Hayashi fig. 4 # 56, col. 5 lines 66, and lines 30-47).

where M1 is selected from a group consisting of Au, Pat, IR, PD,OS, Re, Rh, Tu, Cu,Co,Fe, Ni,V and Cr (Hayashi col. 5 line 29) and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W,Y, Mo and Nb. (Hayashi col. 5 line 44-45).

With respect to claim 2, wherein the composition ratio of said barrier layer is directed so that grain boundary becomes amorphous to an extend such that at least any one of diffusion of oxygen and spike can be prevented. (Hayashi col. 12 lines 15-22).

With respect to claim 3, wherein the surface of semiconductor substrate is a tungsten plug formed on the semiconductor substrate (Hayashi fig.4 , col.6 lines 1-3).

With respect to claim 4, wherein the surface of semiconductor substrate is formed by material which promotes oxidation at crystallization temperature of a dielectric layer to be formed on said surface of semiconductor. (Hayashi Si –substrate and dielectric SiO_2).

With respect to claim 5, wherein the surface of the semiconductor substrate is formed by at least one kind of polysilicon, tungsten, cobalt, molybdenum, cooper, silicide of these and alloy of these (Hayashi col. 3 line 40).

With respect to claim 6, wherein a dielectric layer is formed on said surface of electrode. (Hayashi col.3 line 42) .

With respect to claim 7, wherein the dielectric layer is PZT. (Hayashi col. 4 line 6).

With respect to claim 8, wherein a lower electrode formed on a semiconductor substrate (Hayashi fig.4 #73, col. 5 line 64), a dielectric layer formed on the lower electrode and constructed by ferro electric or dielectric having high dielectric constant (fig. 4 # dielectric surrounding 73) and an upper electrode formed on said dielectric layer (Hayashi fig. 4 # 60 formed on substrate 51, col. 5 lines 65-67) wherein said electrode includes a barrier layer consisting of amorphous or micro crystal expressed by an expression of M1 M2 (Hayashi fig. 4 # 56, col. 5 lines 66, and lines 30-47).

where M1 is selected from a group consisting of Au, Pat, IR, PD,OS, Re, Rh, Tu, Cu,Co,Fe, Ni,V and Cr (Hayashi col. 5 line 29) and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W,Y, Mo and Nb. (Hayashi col. 5 line 44-45).

With respect to claim 13, wherein a lower electrode formed on a semiconductor substrate (Hayashi fig.4 #73, col. 5 line 64), a dielectric layer formed on the lower electrode and constructed by ferro electric or dielectric having high dielectric constant (fig. 4 # dielectric surrounding 73) and an upper electrode formed on said dielectric layer (Hayashi fig. 4 # 60 formed on substrate 51, col. 5 lines 65-67) wherein said electrode includes between said dielectric layer and said upper electrode a barrier layer consisting of amorphous or micro crystal expressed by an expression of $M1_xM2_{1-x}$ ($0 < x < 1$), (Hayashi fig. 4 # 56, col. 5 lines 66, and lines 30-47).

where M1 is selected from a group consisting of Au, Pat, IR, PD,OS, Re, Rh, Tu, Cu,Co,Fe, Ni,V and Cr (Hayashi col. 5 line 29) and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W,Y, Mo and Nb. (Hayashi col. 5 line 44-45).

wherein said electrode includes a barrier layer consisting of amorphous or micro crystal expressed by an expression of M1 M2 (Hayashi fig. 4 # 56, col. 5 lines 66, and lines 30-47).

With respect to claim 15, wherein Hayashi describes a semiconductor device having an electrode formed on a surface of a semiconductor substrate, (Hayashi fig. 4 # 60 formed on substrate 51, col. 5 lines 65-67) wherein said electrode includes amorphous or micro crystal single layer expressed by an expression of $M1_x M2_{1-x}$ ($0 < x < 1$), (Hayashi fig. 4 # 56, col. 5 lines 66, and lines 30-47).

where M1 is selected from a group consisting of Au, Pat, IR, PD,OS, Re, Rh, Tu, Cu,Co,Fe, Ni,V and Cr (Hayashi col. 5 line 29) and M2 is selected from a group consisting of Ta, Ti, Zr, Hf, W,Y, Mo and Nb. (Hayashi col. 5 line 44-45).

With respect to claim 16, wherein the barrier layer includes of constructive element of substrate material. (Hayashi col. Col. 5 lines 29-30).

With respect to claim 31, wherein a lower electrode formed on a semiconductor substrate (Hayashi fig.4 #73, col. 5 line 64), wherein said electrode includes at least an element chosen from a first group of Au, Pat, IR, PD,OS, Re, Rh, Tu, Cu,Co,Fe, Ni,V and Cr (Hayashi col. 5 line 29) and at least an element chosen from a second group of Ta, Ti, Zr, Hf, W,Y, Mo and Nb. (Hayashi col. 5 line 44-45).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-12 , 14 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al. (U.S. Patent No. 6,133,092 herein after Hayashi) as applied to claims 1-8 ,etc. above and further in view of Xing (U.S. patent No. 6,492,222 Herein after Xing).

With respect to claim 9, wherein the barrier layer consists of iridium tantalum layer Ir_xTa_{1-x} ($o<x<1$).

Hayashi does not specifically teach or disclose the barrier layer as consisting of Ir_xTa.

However Xing, a patent from the same filed of endeavor, describes in col. 9 lines 10 a barrier layer of Ir_xTa_{1-x} ($o<x<1$) to form a layer of noble metal that is stable in oxygen and further to minimize degradation against fatigue.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use Xing's Ir_xTa_{1-x} instead of the other materials taught by Hayashi in Hayashi's device .The motivation to make above mentioned substitution is to form a layer of noble metal that is stable in oxygen and further to minimize degradation against fatigue. (Xing col. 9 lines 7, and col. 610 lines 15-17).

With respect to claim 10, wherein the barrier layer includes a grading layer in which a composition ratio is changed. (Hayashi fig. 5, col. 6 lines 50-55).

With respect to claim 11, wherein the barrier layer consists of iridium tantalum layer Ir_xTa_{1-x} (o<x<1). (Hayashi col. 3 lines 50-56- grading layer, Xing col.9 line 10) and the material of the electrode is iridium (Xing col. 9 line 10) .

With respect to claim 12, wherein the barrier layer consists of iridium tantalum layer Ir_xTa_{1-x} (o<x<1). (Hayashi col. 3 lines 50-56, Xing col.9 line 10) and the material of the electrode is platinum. (Xing col. 9 line 9) .

With respect to claim 14, wherein the barrier layer consists of iridium tantalum layer Ir_xTa_{1-x} (o<x<1). (Hayashi col. 3 lines 50-56, Xing col.9 line 10).

With respect to claim 32, wherein the barrier layer is made of IrTaPt. (Xing col.9 lines 9-11).

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Steven H. Rao

Patent Examiner

December 13, 2002.

SUPERVISORY PRIMARY EXAMINER
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